1. An integrated circuit comprising:

a first conductor and a second conductor having different first and second spans, respectively, in a first dimension, wherein said first span has a greater span than said second span;

at least one conductor of said first conductor and said second conductor selectively coupled to two independently controlled first and second switches, wherein a first program controlled logic cell drives said at least one conductor through at least said first switch and a second program controlled logic cell drives said at least one conductor through at least said second switch; and

wherein said first span is selectively coupled to drive said second span through a third switch without requiring traversal of another span, wherein said first span and said second span are spanning at least one common program controlled logic cell in the first dimension.

2. The integrated circuit as set forth in claim 1, wherein said switches comprise program controlled passgates.

3. The integrated circuit as set forth in claim 1, wherein said switches comprise program controlled drivers/receivers.

4. The integrated circuit as set forth in claim 1, wherein said switches comprise program controlled passgates and program controlled drivers/receivers.

5. The integrated circuit as set forth in claim 1, wherein at least one of said switches has a program controlled on state and off state.

6. The integrated circuit as set forth in claim 1, wherein said integrated circuit is implemented using process technology incorporating memory devices.

7. The integrated circuit as set forth in claim 1, wherein said integrated circuit is implemented using process technology incorporating non-volatile memory devices.

8. The integrated circuit as set forth in claim 1, wherein said integrated circuit is implemented using process technology incorporating fuse devices.

9. The integrated circuit as set forth in claim 1, wherein said integrated circuit is implemented using process technology incorporating anti-fuse devices.

10. The integrated circuit as set forth in claim 1, wherein said integrated circuit is implemented using process technology incorporating ferro-electric devices.

11. The integrated circuit as set forth in claim 1, further comprises a third conductor having a third span.

12. The integrated circuit as set forth in claim 11, wherein said third span selectively couples to said first span through a fourth switch without requiring traversal of another span.

13. The integrated circuit as set forth in claim 12, wherein said second span is equal to said third span and said third span is in the first dimension.

14. The integrated circuit as set forth in claim 13, wherein said second span is spanning at least one different program controlled logic cell than said third span in the first dimension.

15. The integrated circuit as set forth in claim 11, wherein said third span is in a second dimension.

16. The integrated circuit as set forth in claim 15, wherein said third span selectively couples to at least one span of said first span and said second span through a fifth switch without requiring traversal of another span.

17. The integrated circuit as set forth in claim 16, wherein said third span is equal in span to said at least one span.

18. The integrated circuit as set forth in claim 11, wherein said first span, said second span and said third span are three different spans in the first dimension.

19. The integrated circuit as set forth in claim 18, wherein said second span selectively couples to said third span through a sixth switch without requiring traversal of another span.

20. The integrated circuit as set forth in claim 18, further comprises at least three conductors having three different spans in a second dimension.

21. The integrated circuit as set forth in claim 20, wherein at least one span of said three different spans in the second dimension selectively couples to at least one span of said first, second and third spans through a switch without requiring traversal of another span.

22. The integrated circuit as set forth in claim 19, further comprising a fourth conductor having a fourth span, wherein said fourth span selectively couples to at least one span of said

first span, said second span and said third span through a seventh switch without requiring traversal of another span.

23. The integrated circuit as set forth in claim 22, wherein said fourth span is in one of a dimension of a group consisting of said first dimension and said second dimension.

24. A method of providing an integrated circuit comprising:

providing a first conductor and a second conductor having different first and second spans, respectively, in a first dimension, wherein said first span has a greater span than said second span;

selectively coupling at least one conductor of said first conductor and said second conductor to two independently controlled first and second switches, wherein a first program controlled logic cell drives said at least one conductor through at least said first switch and a second program controlled logic cell drives said at least one conductor through at least said second switch; and

selectively coupling said first span to drive said second span through a third switch without requiring traversal of another span, wherein said first span and said second span are spanning at least one common program controlled logic cell in the first dimension.

25. The method as set forth in claim 24, further comprises providing a third conductor having a third span.

26. The method as set forth in claim 25, wherein said third span selectively couples to said first span through a fourth switch without requiring traversal of another span.

27. The method as set forth in claim 26, wherein second span is equal to said third span and said third span is in the first dimension.

28. The method as set forth in claim 27, wherein second span spans at least one different program controlled logic cell than said third span in the first dimension.

29. The method as set forth in claim 25, wherein said third span is in a second dimension.

30. The method as set forth in claim 29, further comprising selectively coupling said third span to at least one span of said first span and said second span through a fifth switch without requiring traversal of another span.

31. The method as set forth in claim 30, wherein said third span is equal in span to said at least one span.

32. The method as set forth in claim 25, wherein said first span, said second span and said third span are three different spans in said first dimension.

33. The method as set forth in claim 32, further comprising selectively coupling said second span to said third span through a sixth switch without requiring traversal of another span.

34. The method as set forth in claim 32, further comprising providing at least three different conductors having three different spans in a second dimension.

35. The method as set forth in claim 34, wherein at least one span of said three different spans in the second dimension selectively couples to at least one span of said first, second and third spans through a switch without requiring traversal of another span.

36. The method as set forth in claim 33, further comprising providing a fourth conductor having a fourth span, wherein said fourth span selectively couples to at least one span of said first span, said second span and said third span through a seventh switch without requiring traversal of another span.

37. The method as set forth in claim 36, wherein said fourth span is in one of a dimension of a group consisting of said first dimension and said second dimension.

38. An integrated circuit comprising:

a first conductor and a second conductor having a different first and second spans, respectively, in a first dimension, wherein said first span and said second span are spanning at least one common program controlled logic cell in the first dimension;

a third conductor having a third span in a second dimension;

said first span selectively couples to said third span through a first switch without requiring traversal of another span and said second span selectively couples to said first span through a second switch without requiring traversal of any other span; and

at least one conductor of said first conductor, said second conductor and said third conductor selectively couples to two independently controlled third and fourth switches, wherein a first program controlled logic cell drives said at least one

conductor through at least said third switch and a second program controlled logic cell drives said at least one conductor through at least said fourth switch.

39. The integrated circuit as set forth in claim 38, wherein said first span is greater than said second span.

40. The integrated circuit as set forth in claim 38, wherein said second span is greater than said first span.

41. The integrated circuit as set forth in claim 40, further comprising a fourth conductor having a fourth span in the first dimension, wherein said fourth span is greater than said second span.

42. The integrated circuit as set forth in claim 41, wherein said switches comprise program controlled passgates.

43. The integrated circuit as set forth in claim 41, wherein said switches comprise program controlled drivers/receivers.

44. The integrated circuit as set forth in claim 41, wherein said switches comprise program controlled passgates and program controlled drivers/receivers.

45. The integrated circuit as set forth in claim 41, wherein at least one of said switches has a program controlled on state and off state.

46. The integrated circuit as set forth in claim 41, wherein said integrated circuit is implemented using process technology incorporating memory devices.

47. The integrated circuit as set forth in claim 41, wherein said integrated circuit is implemented using process technology incorporating non-volatile memory devices.

48. The integrated circuit as set forth in claim 41, wherein said integrated circuit is implemented using process technology incorporating fuse devices.

49. The integrated circuit as set forth in claim 41, wherein said integrated circuit is implemented using process technology incorporating anti-fuse devices.

50. The integrated circuit as set forth in claim 41, wherein said integrated circuit is implemented using process technology incorporating ferro-electric devices.

51. The integrated circuit as set forth in claim 41, wherein said fourth span selectively couples said second span through a fifth switch.

52. A method of providing an integrated circuit comprising:

providing a first conductor and a second conductor having a different first and second spans, respectively, in the first dimension, wherein said first span and said second span are spanning at least one common program controlled logic cell;

providing a third conductor having a third span in a second dimension;

selectively coupling said first span to said second span through a first switch without requiring traversal of another span;

selectively coupling said first span to said second span through a second switch without requiring traversal of any other span; and

selectively coupling at least one conductor of said first conductor, said second conductor and said third conductor to two independently controlled third and fourth switches, wherein a first program controlled logic cell drives said at least one conductor through at least said third switch and a second program controlled logic cell drives said at least one conductor through at least said fourth switch.

53. The method as set forth in claim 52, wherein said first span is greater than said second span.

54. The method as set forth in claim 52, wherein said second span is greater than said first span.

55. The method as set forth in claim 54, further comprising providing a fourth conductor having a fourth span in said first dimension, wherein said fourth span is greater than said second span.

56. The method as set forth in claim 55, further comprising selectively coupling said fourth span to said second span through a fifth switch.